Massively parallel multicanonical simulations on GPUs

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Computational Quantum Field Theory

Outline

Timeline of generalized ensemble techniques

These advanced Monte Carlo technique are designed to estimate the density of states.

- 1986 - Replica-exchange (Swendsen, Wang)
- 1989 - Multiple histogram reweighting (Ferrenberg, Swendsen)
- 1991 - Parallel tempering (Geyer; 1996 Hukushima, Nemoto)
- 1992 - Multicanonical (MUCA) sampling (Berg, Neuhaus)
- 2001 - Wang-Landau sampling (Wang, Landau)
- 2013 - Parallel MUCA (Zierenberg, Marenz, Janke) (few cores)

Now we expand the parallel MUCA algorithm to tens of thousands of cores.

Parallel multicanonical weight iteration

The canonical partition sum can be rewritten in terms of the density of states $\Omega(E)$

$$\mathcal{Z}_{\rm can} = \sum_E \Omega(E) e^{-\beta E} \rightarrow \mathcal{Z}_{\rm muca} = \sum_E \Omega(E) W(E)$$

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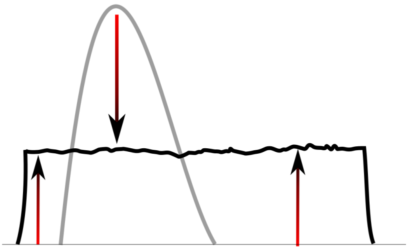

Figure: Flat histogram

For a flat histogram $W(E) \propto \Omega^{-1}(E)$. Since the density of states is usually not known in advance, the weights have to be determined iteratively.

Parallel multicanonical weight iteration

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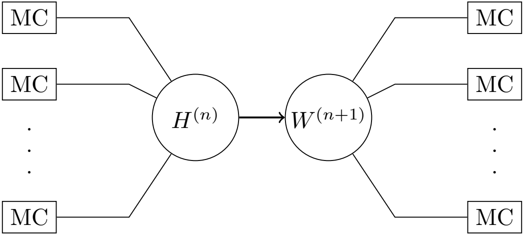

Figure: Parallel multicanonical simulation scheme

$$\sum_i H_i^{(n)}(E) = H^{(n)}(E) \rightarrow W^{(n+1)}(E) = W_i^{(n+1)}(E)$$

with

$$W^{(n+1)}(E) = \frac{W^{(n)}(E)}{H^{(n)}(E)}$$

Hardware overview

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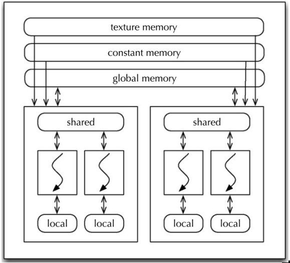
	CPU	GPU1	GPU2
model	2× Xeon E5-2640	Tesla K20m (ECC)	GTX Titan Black
peak clock speed	3072 MHz	706 MHz	980 MHz
# cores	12 (24 w/ HT)	2496	2880
SMX	N/A	13	15
memory bandwidth	42.6 GB/s	208 GB/s	336 GB/s
peak performance	2× 120 GFlop/s	3.5 TFlop/s	5.1 TFlop/s
thermal design power	2×95 W	225 W	250 W

Table: List of considered CPU and GPU hardware with selected properties, including the clock speed, the number of total cores, the number of streaming multiprocessors (SMX), the memory bandwidth and the power consumption (thermal design power TDP). Both GPUs are from the Kepler generation such that each SMX features 192 cores.

GPU architecture

- GPGPUs specifically designed for HPC
- but also gaming PC GPUs can be used
- features streaming multiprocessors (SMX) with multiple cores
- currently $\sim$ 2500 to 3000 cores in total
- available memory typically 6 GB to 12 GB
- programmed using CUDA, a subset of C99/C++
- you have to optimize your code for different layers of memory
- overload cores with many threads to hide memory latency (get optimal number of worker threads using CUDA occupancy calculator)



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This implementation ensures identical timeseries and histograms for CPU and GPU, if parameters are the same (number of workers and seeds, specifically).

Simulational parameters

Each weight iteration:

- NUPDATES_THERM $= \min(100, 30 \cdot \text{width})$
- while (width $<$ N)
  NUPDATES_MEASURE $= 6 \cdot \text{width}^{2.25}$/NUM_WORKERS
- NUPDATES_MEASURE *= 1.1 **until flat**

Production run:

- thermalization with NUPDATES_THERM $= N^{2.25}$
- NUPDATES_MEASURE calculated from spinflip times to set fixed runtime (10 min)

width - width of energy range covered
$N = L^2$ - full energy range
L - lattice size
NUPDATES_THERM - number of thermalization updates (spin flips)
NUPDATES_MEASURE - number of measurement updates

J. Zierenberg et. al, CPC 184 1155 (2013).

How to tell if your histogram is flat?

- Most flat histogram methods stop the iteration when the histogram is "flat enough".
  As an example we aim for 80% flatness in our histogram, that means if $0.8 \cdot h_{\text{mean}} \leq H(E) \leq h_{\text{mean}}/0.8 \quad \forall E$, with $h_{\text{mean}} = \frac{1}{N_M} \sum H(E)$ our histogram is flat.
- Related to Chebyshev distance

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- Kullback-Leibler divergence, measure of difference between two probability distributions P and Q
- $d_k = \sum_i P(i) \log \frac{P(i)}{Q(i)}$
- in our implementation we use
  $P(i) = H(E)/\text{NUPDATES\_MEASURE}$ and $Q(i) = 1/\text{NUM\_BINS}$

Thermalization

Influence of the number of thermalization steps on the converge of the Kullback-Leibler divergence.

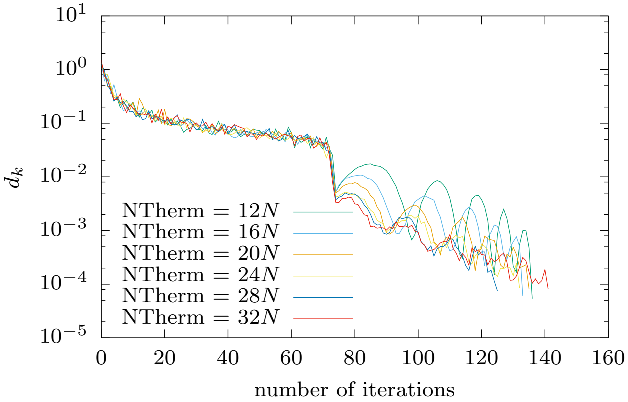


Figure: Kullback-Leibler divergence as function of iterations.

Hardware performance

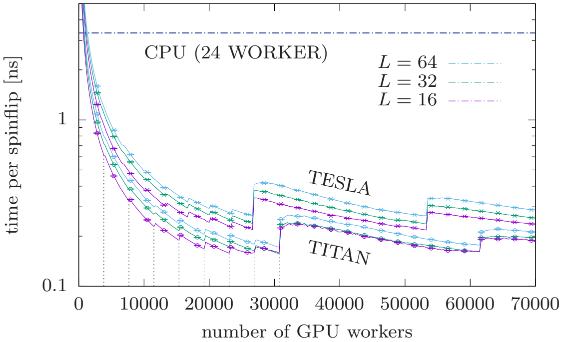
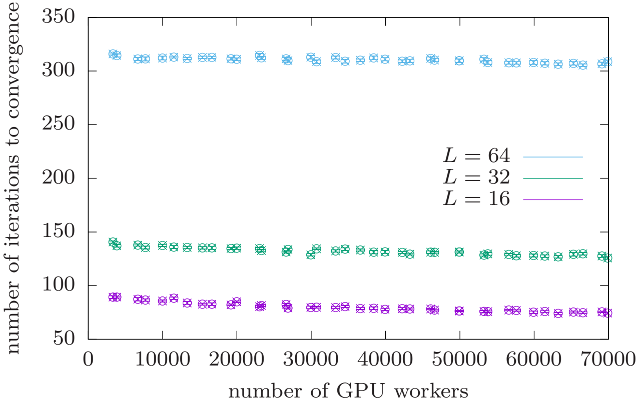


Figure: Hardware performance: spin flip times in ns as function of number of workers.

Average CPU spin flip time similar for all system sizes $t_{CPU} \approx 3.5\,\text{ns}$.
Optimal GPU spin flip times – Tesla: 0.21 ns Titan: 0.16 ns
This results in theoretical hardware speedups of factors of 16 and 21, respectively.

Iterations until convergence



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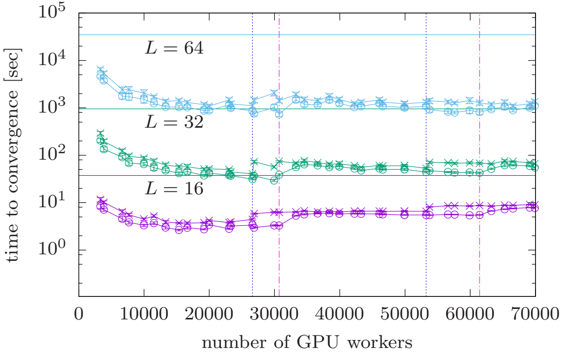
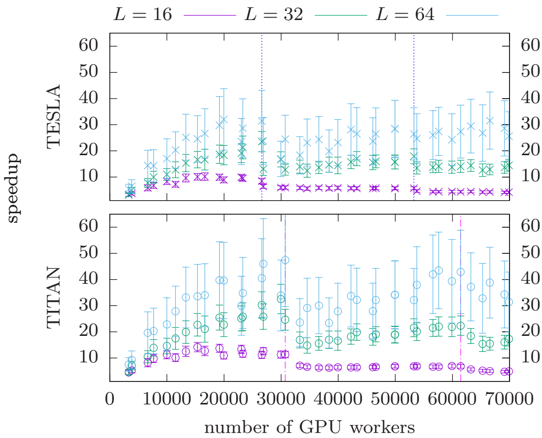
Time to convergence



- solid horizontal lines represent CPU reference times
- vertical dashed lines mark full GPU utilization

Speedup

Software speedup defined by the ratio of CPU and GPU time to convergence.



Density of states

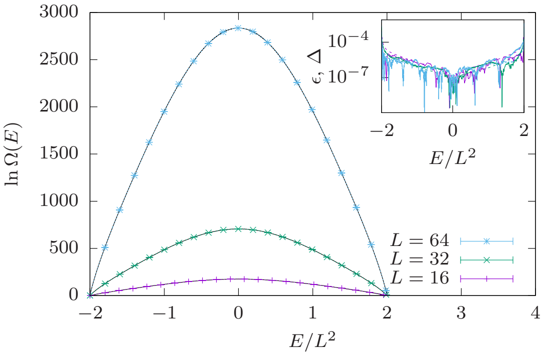


Figure: Density of states for the 2D Ising model obtained from simulation in comparison with exact solution from Beale. The inset shows the deviation of our simulational results from the Beale solution as well as Jackknife errors.

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- Extension to multiple GPUs should be straight-forward

Thank you for your attention.

Funding:

Polymers under multiple constraints